WHAT IS CLAIMED IS

1. A parallel processor comprising:

a global processor interpreting a program and controlling the entirety of the processor; and

a processor-element block comprising a plurality of processor elements each comprising a register file and an operation array for processing a plurality of sets of data,

wherein said global processor outputs a control signal to said plurality of processor elements, and, thereby, sets processor-element numbers corresponding to said plurality of processor elements as input values of the operation arrays, respectively.

2. The processor as claimed in claim 1, wherein data from a general-purpose register of said global processor is transferred to arbitrary processor elements of said plurality of processor elements.

3. The processor as claimed in claim 2, wherein the data transfer is rendered through specifying a range from a first specific processor element through a second specific processor element by specifying immediate values by using operands.

4. The processor as claimed in claim 2, wherein the data transfer is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation; and specifying processor elements by masking arbitrary bits of the thus-specified bits, through specifying the immediate values by using the operands.

5. The processor as claimed in claim 2, wherein the data transfer is rendered through specifying by a pointer using a general-purpose register of said global processor.

6. The processor as claimed in claim 5, wherein the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying.

7. The processor as claimed in claim 1, wherein each processor element comprises a plurality of flag bits for controlling, according to a state of the data, as to whether or not the operation processing is to be executed, according to whether or not a condition is satisfied, and, renders AND/OR operation on a specific bit of said flag bits.

8. The processor as claimed in claim 7, wherein specifying of said flag bits is rendered by specifying the range from the first specific processor element through the second specific processor element through specifying the immediate values by using the operands.

9. The processor as claimed in claim 7, wherein specifying of said flag bits is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation; and specifying processor elements by masking arbitrary bits of the thus-specified bits through specifying the immediate values by using the operands.

10. The processor as claimed in claim 7, wherein specifying of said flag bits is rendered through specifying by a pointer using a general-purpose register of said global processor.

11. The processor as claimed in claim 10, wherein the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying.

12. A parallel processor comprising:

a global processor interpreting a program and controlling the entirety of said processor; and

a processor-element block comprising a plurality of processor elements each processing data, wherein:

each processor element comprises an operation part, a register file comprising a plurality registers and an operation-result flag; and

data from a table memroy is stored in at least one register of each of a plurality of processor elements having the same contents of the operation-result flag, simultaneously.

13. The processor as claimed in claim 12, wherein:

in each processor element, the operation part compares data to undergo the operation with data to be converted, and, when the data to undergo the operation coincides with the data to be converted, sets a flag as condition satisfaction to the operation-result flag; and

the data after conversion from said table

memroy is stored in the at least one register of each of the plurality of processor elements having the same contents of the operation-result flag, simultaneously.

14. The processor as claimed in claim 12, wherein:

in each processor element, the operation part compares data to undergo the operation with data to be converted, and, when the data to undergo the operation is larger than the data to be converted, sets a flag as condition satisfaction to the operation-result flag; and

the data after conversion from said table memroy is stored in the at least one register of each of the plurality of processor elements having the same contents of the operation-result flag. simultaneously.

15. The processor as claimed in claim 12, wherein:

a data transfer bus connecting said table

memroy to the register of said register file of each processor element, and a control part controlling data transfer from said data transfer bus to said register are provided; and

said control part stores data into said register from said data transfer bus according to a control signal from said global processor and the condition of said operation-result flag.

16. The processor as claimed in claim 15, wherein the data after conversion comprises data after conversion corresponding to successive 2^n sets of data to be converted, and is written to 2^n registers from 2^n table data buses simultaneously, where n denotes an integer.

17. The processor as claimed in claim 12, wherein a plurality of registers, built in each processor element, which can store data from a table

memory simultaneously, can also be used for storing data to undergo operation processing in each processor element.

18. The processor as claimed in claim 12, wherein data of a table memory to be stored in a plurality of registers is stored in a memory built in said global processor, and said memroy can also be used as a memory for storing data processed in operation of said global processor.

19. An image processing apparatus, comprising:

an input FIFO and an output FIFO; and

a parallel processor comprising a plurality of processor elements which form an array configuration, wherein:

image data is input to said processor via said input FIFO;

said processor processes the image data in parallel; and

data having undergone operation processing performed by said processor is output via said output FIFO,

wherein:

each processor element of said processor comprises an operation part, a register file comprising a plurality of registers, and an operation-result flag;

data after conversion for non-linear processing from a table memroy is stored in at least one register of each of a plurality of processor elements having the same contents of the operation-result flag, simultaneously; and

the image data having undertone the non-linear processing is output externally.

20. The image processing apparatus as claimed in claim 19, wherein:

in each processor element, the operation part compares data to undergo the operation with data to be converted, and, when the data to undergo the operation

is larger than the data to be converted, sets a flag as condition satisfaction to the operation-result flag; and

data after conversion from said table memroy is stored in the at least one register of each of the plurality of processor elements having the same contents of the operation-result flag, simultaneously.

21. The image processing apparatus as claimed in claim 19, wherein:

a data transfer bus connecting said table memroy to the register of said register file of each processor element, and a control part controlling data transfer from said data transfer bus to said register are provided; and

said control part stores data into said register from said data transfer bus according to a control signal from said global processor and the condition of said operation-result flag.

22. The image processing apparatus as claimed in clam 21, wherein the data after conversion comprises data after conversion corresponding to successive 2^n sets of data to be converted, and are written to 2^n registers from 2^n table data buses simultaneously, where n denotes an integer.